



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

AF \$X
2814

Applicant: Nobutoshi AOKI et al.

Attorney Docket 40301/0578

Title: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING
INSULATED GATE FIELD EFFECT TRANSISTOR AND METHOD
OF MANUFACTURING THE SAME

Appl. No.: 09/440,928

Filing Date: November 16, 1999

Examiner: S. Rao

Art Unit: 2814

RECEIVED
TECHNOLOGY CENTER 2800
OCT -4 2002TRANSMITTALCommissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment and Reply in the above-captioned application. The fee has been calculated as shown below. (*Small entity fees indicated in parentheses.*)

CLAIMS AS AMENDED						
(1)	(2)	(3)	(4)	(5)	(6)	(7)
	Claims Remaining After Amendment		Highest Number Previously Paid For	Extra Claims	Rate	Fee
Total Claims	31	-	31	0	18.00	
(Small Entity)					(9.00)	
Independent claims	10	-	10	0	84.00	
(Small Entity)					(42.00)	
Multiple Dependent		-			280.00	
(Small Entity)					(140.00)	
Extension of Time		One Month	Two Months	Three Months	Four Months	
Fee	\$110		\$400	\$920	\$1,440	\$110.00
(Small Entity)	(\$55)		(\$200)	(\$460)	(\$720)	
Total Fees						\$110.00

A check in the amount of the above Total Fees is attached. This amount is believed to be correct; however, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 19-0741.

Respectfully submitted,

Aaron C. Chatterjee
Reg. No. 41,398

Date: September 30, 2002

FOLEY & LARDNER
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(202) 672-5300

002.899323.1



Attorney Docket 040301-0578

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DO MD #10/C
Geoff Geffen
10/10/02
marsh a
10/10/02

AMENDMENT AND REPLY UNDER 37 C.F.R. § 1.116

Commissioner for Patents
Washington, D.C. 20231
BOX AF

Sir:

In reply to the Office Action mailed May 31, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims by replacing the indicated claims with the following clean version. (See Attachment A for the marked up version of the amended claims.)

- (X) gss d*
1. (Three Times Amended) A semiconductor device comprising:
a pair of main electrodes used as source and drain electrodes;
an insulating gate film adjacent to the pair of main electrodes; and
a gate electrode comprising of a first region including at least a first group IV element and a second group IV element and formed in contact with the insulating gate film, and a second region including the first group IV element and formed on the first region, the first region and the second region having an identical conductivity type.